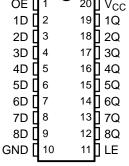


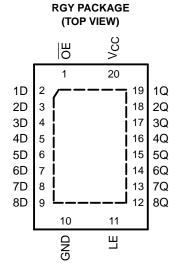
### **FEATURES**

- Inputs Are TTL-Voltage Compatible
- 4.5-V to 5.5-V V<sub>CC</sub> Operation
- Typical  $t_{pd} = 5.1 \text{ ns at 5 V}$
- Typical V<sub>OLP</sub> (Output Ground Bounce) <0.8 V at  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^{\circ}\text{C}$
- Typical  $V_{OHV}$  (Output  $V_{OH}$  Undershoot) >2.3 V at  $V_{CC}$  = 5 V,  $T_A$  = 25°C
- **Supports Mixed-Mode Voltage Operation on All Ports**

DB, DGV, DW, NS, OR PW PACKAGE (TOP VIEW) 20 V<sub>CC</sub> ΟE



- I<sub>off</sub> Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 250 mA Per **JESD 17**
- **ESD Protection Exceeds JESD 22** 
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)



### **DESCRIPTION/ORDERING INFORMATION**

The SN74LV573AT is an octal transparent D-type latch. When the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is low, the Q outputs are latched at the logic levels of the D inputs.

### ORDERING INFORMATION

T <sub>A</sub>	PA	CKAGE <sup>(1)</sup>	ORDERABLE PART NUMBER	TOP-SIDE MARKING		
	QFN – RGY	Tape and reel	SN74LV573ATRGYR	VV573		
	SOIC - DW	Tube	SN74LV573ATDW	LV573AT		
	3010 - 000	Tape and reel	SN74LV573ATDWR	LVS/SAT		
–40°C to 85°C	SOP – NS Tape and reel		SN74LV573ATNSR	74LV573AT		
-40°C 10 85°C	SSOP – DB	Tape and reel	SN74LV573ATDBR	LV573AT		
	TSSOP – PW	Tube	SN74LV573ATPW	LV573AT		
	1550P – PW	Tape and reel	SN74LV573ATPWR	LV5/3AT		
	TVSOP - DGV	Tape and reel	SN74LV573ATDGVR	LV573AT		

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



# **DESCRIPTION/ORDERING INFORMATION (CONTINUED)**

A buffered output-enable  $(\overline{OE})$  input can be used to place the eight outputs in either a normal logic state (high or low) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.

To ensure the high-impedance state during power up or power down,  $\overline{\text{OE}}$  shall be tied to  $V_{\text{CC}}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

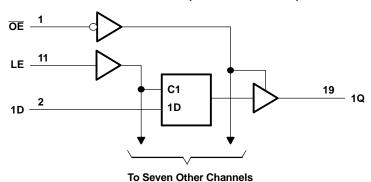
OE does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

This device is fully specified for partial-power-down applications using I<sub>off</sub>. The I<sub>off</sub> circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

# FUNCTION TABLE (EACH LATCH)

	INPUTS	OUTPUTS	
ŌĒ	LE	D	Q
L	Н	Н	П
L	Н	L	L
L	L	X	$Q_0$
Н	X	X	Z

### **LOGIC DIAGRAM (POSTIVE LOGIC)**





# Absolute Maximum Ratings<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT	
$V_{CC}$	Supply voltage range		-0.5	7	V	
$V_{I}$	Input voltage range (2)		-0.5	7	V	
Vo	Voltage range applied to any output in the high-impedance	e or power-off state (2)	-0.5	7	V	
Vo	Output voltage range applied in the high or low state (2)(3)		-0.5	V <sub>CC</sub> + 0.5	V	
I <sub>IK</sub>	Input clamp current	V <sub>I</sub> < 0		-20	mA	
I <sub>OK</sub>	Output clamp current	V <sub>O</sub> < 0		-50	mA	
Io	Continuous output current	$V_O = 0$ to $V_{CC}$		±35	mA	
	Continuous current through V <sub>CC</sub> or GND		±70	mA		
		DB package (4)		70		
		DGV package <sup>(4)</sup>		92		
0	Deckage thermal impedance	DW package <sup>(4)</sup>		58	°C/W	
$\theta_{JA}$	Package thermal impedance	NS package (4)		60		
		PW package <sup>(4)</sup>		83	•	
		RGYpackage <sup>(5)</sup>				
T <sub>stg</sub>	Storage temperature range		-65	150	°C	

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) This value is limited to 5.5 V maximum.
- 4) The package thermal impedance is calculated in accordance with JESD 51-7.
- (5) The package thermal impedance is calculated in accordance with JESD 51-5.

# Recommended Operating Conditions<sup>(1)</sup>

			MIN	MAX	UNIT
$V_{CC}$	Supply voltage		4.5	5.5	V
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 4.5 V to 5.5 V	2		V
V <sub>IL</sub>	Low-level input voltage	V <sub>CC</sub> = 4.5 V to 5.5 V		0.8	V
VI	Input voltage		0	5.5	V
V	Output voltage		0	$V_{CC}$	V
Vo	Output voltage	3-state	0	5.5	V
I <sub>OH</sub>	High-level output current	V <sub>CC</sub> = 4.5 V to 5.5 V		-16	mA
I <sub>OL</sub>	Low-level output current	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$		16	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$		20	ns/V
T <sub>A</sub>	Operating free-air temperature		-40	85	°C

All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

# SN74LV573AT OCTAL TRANSPARENT D-TYPE LATCH WITH 3-STATE OUTPUTS

SCES574C-JUNE 2004-REVISED AUGUST 2005



### **Electrical Characteristics**

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>cc</sub>	T	( = 25°C		T <sub>A</sub> = -	40°C 5°C	UNIT
			MIN	TYP	MAX	MIN	MAX	
V	$I_{OH} = -50 \mu A$	4.5 V	4.4	4.5		4.4		V
V <sub>OH</sub>	$I_{OH} = -16 \text{ mA}$	4.5 V	3.8	3.8 3.8 0 0.1 0.1 0.1 0.55 0.55 ±0.1 ±1	V			
V <sub>OL</sub>	$I_{OL} = 50 \mu A$	4.5 V		0	0.1		0.1	V
V OL	I <sub>OL</sub> = 16 mA	4.5 V			0.55		0.55	V
I <sub>I</sub>	$V_I = 5.5 \text{ V or GND}$	0 to 5.5 V			±0.1		±1	μΑ
I <sub>OZ</sub>	$V_O = V_{CC}$ or GND	5.5 V			±0.25		±2.5	μΑ
I <sub>CC</sub>	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V			2		20	μΑ
$\Delta I_{CC}^{(1)}$	One input at 3.4 V, Other inputs at V <sub>CC</sub> or GND	5.5 V			1.35		1.5	mA
I <sub>off</sub>	$V_I$ or $V_O = 0$ to 5.5 V	0			0.5		5	μΑ
C <sub>i</sub>	$V_I = V_{CC}$ or GND			4.5				pF

<sup>(1)</sup> This is the increase in supply current for each input at one of the specified TTL voltage levels, rather than 0 V or V<sub>CC</sub>.

### **Timing Requirements**

over recommended operating free-air temperature range,  $V_{CC}$  = 5 V  $\pm$  0.5 V (unless otherwise noted) (see Figure 1)

		T <sub>A</sub> = 2	T <sub>A</sub> = 25°C		T <sub>A</sub> = -40°C to 85°C		
		MIN	MAX	MIN	MAX		
t <sub>w</sub>	Pulse duration, LE high	6.5		8.5		ns	
t <sub>su</sub>	Setup time, data before LE↓	1.5		1.5		ns	
t <sub>h</sub>	Hold time, data after LE $\downarrow$	3.5		3.5		ns	

### **Switching Characteristics**

over recommended operating free-air temperature range,  $V_{CC}$  = 5 V  $\pm$  0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM	TO (OUTPUT)	LOAD	т,	<sub>A</sub> = 25°C	;	T <sub>A</sub> = -	UNIT		
	(INPUT)	(OUTPUT)	CAPACITANCE	MIN	TYP	MAX	MIN	MAX		
t <sub>PLH</sub>	D	Q	C <sub>L</sub> = 15 pF	2.6	5.1	8.5	1	9.5	20	
t <sub>PHL</sub>	Ь	Q	C <sub>L</sub> = 15 pr	3	5.1	8.5	1	9.5	ns	
t <sub>PLH</sub>	LE	Q	C <sub>L</sub> = 15 pF	3	7.7	12.3	1	14.5	ns	
t <sub>PHL</sub>	LC	Q	C <sub>L</sub> = 15 pr	3.5	7.7	12.3	1	14.5	115	
t <sub>PZH</sub>	ŌĒ	Q	C 15 pF	3	6.3	10.9	1	12.5	20	
t <sub>PZL</sub>	OE	Q	Q $C_L = 15 \text{ pF}$	3.3	6.3	10.9	1	12.5	ns	
t <sub>PHZ</sub>	ŌĒ	0	C <sub>L</sub> = 15 pF	2.8	5.5	8	1	11	ns	
$t_{PLZ}$	OE	Q	OL = 15 pr	1.6	5.4	8	1	9.5		
t <sub>PLH</sub>	<b>D</b>	0	C <sub>L</sub> = 50 pF	3.7	5.9	9.5	1	10.5	ns	
t <sub>PHL</sub>	D	Q		5.5	5.9	9.5	1	10.5		
t <sub>PLH</sub>	LE	0	C	4.3	8.5	13.3	1	14.5	20	
t <sub>PHL</sub>	LE	Q	$C_L = 50 \text{ pF}$	5.9	8.5	13.3	1	14.5	ns	
t <sub>PZH</sub>	ŌĒ	0	C	4.5	7.1	11.9	1	13.5	20	
t <sub>PZL</sub>	OE	Q	$C_L = 50 \text{ pF}$	5.4	7.1	11.9	1	13.5	ns	
t <sub>PHZ</sub>	ŌĒ	0	C 50 pF	3.3	8.8	11.2	1	12	20	
t <sub>PLZ</sub>	UE	Q	$C_L = 50 \text{ pF}$	2.6	8.8	11.2	1	12	ns	
t <sub>sk(o)</sub>			C <sub>L</sub> = 50 pF			1.5		1.5	ns	





# Noise Characteristics<sup>(1)</sup>

 $V_{CC} = 5 \text{ V}, C_L = 50 \text{ pF}$ 

		$T_A = 25^{\circ}C$			UNIT
		MIN	TYP	MAX	UNIT
V <sub>OL(P)</sub>	Quiet output, maximum dynamic V <sub>OL</sub>		1.1	1.5	V
$V_{OL(V)}$	Quiet output, minimum dynamic V <sub>OL</sub>		-1.1	-1.5	V
V <sub>OH(V)</sub>	Quiet output, maximum dynamic V <sub>OH</sub>		4		V
$V_{IH(D)}$	High-level dynamic input voltage	2			V
$V_{IL(D)}$	Low-level dynamic input voltage			8.0	V

<sup>(1)</sup> Characteristics are for surface-mount packages only.

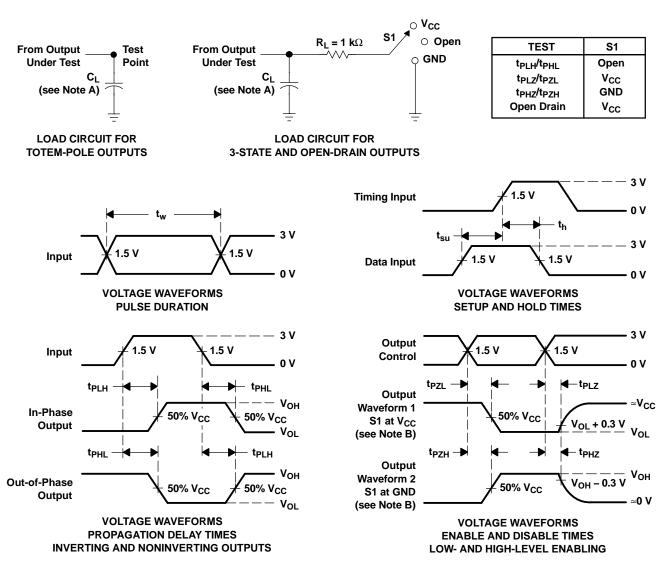
# **Operating Characteristics**

 $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$ 

	PARAMETER	TEST CO	TYP	UNIT		
$C_{pd}$	Power dissipation capacitance	Outputs enabled	$C_L = 50 \text{ pF},$	f = 10 MHz	8	pF



### PARAMETER MEASUREMENT INFORMATION



NOTES: A.  $C_L$  includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  1 MHz,  $Z_O = 50 \Omega$ ,  $t_f \leq$  3 ns.  $t_f \leq$  3 ns.
- D. The outputs are measured one at a time, with one input transition per measurement.
- E. t<sub>PLZ</sub> and t<sub>PHZ</sub> are the same as t<sub>dis</sub>.
- F. t<sub>PZL</sub> and t<sub>PZH</sub> are the same as t<sub>en</sub>.
- G.  $t_{PHL}$  and  $t_{PLH}$  are the same as  $t_{pd}$ .
- H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuits and Voltage Waveforms

20-Aug-2011

#### **PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/ Ball Finish	MSL Peak Temp <sup>(3)</sup>	Samples (Requires Login)
SN74LV573ATDW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LV573ATDWE4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LV573ATDWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LV573ATDWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LV573ATDWRE4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LV573ATDWRG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LV573ATPW	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LV573ATPWE4	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LV573ATPWG4	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LV573ATPWR	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LV573ATPWRE4	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LV573ATPWRG4	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.



### PACKAGE OPTION ADDENDUM

20-Aug-2011

**Pb-Free** (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes. **Pb-Free** (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL. Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

# PACKAGE MATERIALS INFORMATION

www.ti.com 29-Jul-2011

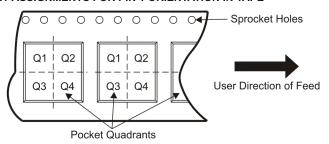
### TAPE AND REEL INFORMATION





	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

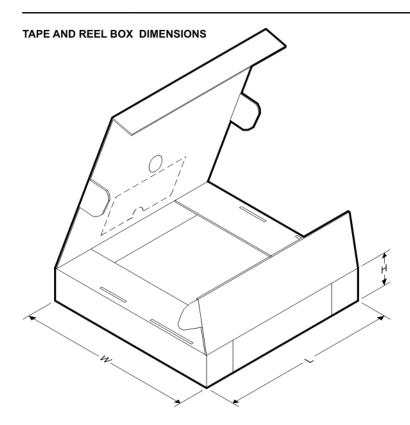


#### \*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LV573ATDWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.0	2.7	12.0	24.0	Q1
SN74LV573ATPWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

**PACKAGE MATERIALS INFORMATION** 

www.ti.com 29-Jul-2011



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LV573ATDWR	SOIC	DW	20	2000	346.0	346.0	41.0
SN74LV573ATPWR	TSSOP	PW	20	2000	346.0	346.0	33.0

DW (R-PDSO-G20)

### PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MS-013 variation AC.



DW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Refer to IPC7351 for alternate board design.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC—7525
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



PW (R-PDSO-G20)

# PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M—1994.
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
- E. Falls within JEDEC MO-153



#### IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Applications

interface.ti.com

Audio www.ti.com/audio Communications and Telecom www.ti.com/communications **Amplifiers** amplifier.ti.com Computers and Peripherals www.ti.com/computers dataconverter.ti.com Consumer Electronics www.ti.com/consumer-apps **Data Converters DLP® Products** www.dlp.com **Energy and Lighting** www.ti.com/energy DSP dsp.ti.com Industrial www.ti.com/industrial Clocks and Timers www.ti.com/clocks Medical www.ti.com/medical

Logic logic.ti.com Space, Avionics and Defense www.ti.com/space-avionics-defense

Security

Power Mgmt power.ti.com Transportation and Automotive www.ti.com/automotive

Microcontrollers microcontroller.ti.com Video and Imaging www.ti.com/video

RFID <u>www.ti-rfid.com</u>
OMAP Mobile Processors www.ti.com/omap

Interface

Wireless Connctivity www.ti.com/wirelessconnectivity

TI E2E Community Home Page <u>e2e.ti.com</u>

www.ti.com/security