SDAS055E - APRIL 1982 - REVISED JULY 1996

- Designed Specifically for High-Speed Memory Decoders and Data Transmission Systems
- Incorporate Three Enable Inputs to Simplify Cascading and/or Data Reception
- Package Options Include Plastic Small-Outline (D) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs

### description

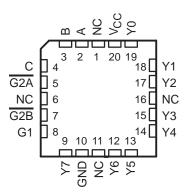
The 'ALS138A and 'AS138 are 3-line to 8-line decoders/demultiplexers designed for highperformance memory-decoding or data-routing applications requiring very short propagation delay times. In high-performance systems, these devices can be used to minimize the effects of emploved decoding. When system with high-speed memories with a fast enable circuit, the delay times of the decoder and the enable time of the memory are usually less than the typical access time of the memory. The effective system delay introduced by the Schottky-clamped system decoder is negligible.

The conditions at the binary-select (A, B, and C) inputs and the three enable (G1,  $\overline{G2A}$ , and  $\overline{G2B}$ ) inputs select one of eight output lines. Two active-low and one active-high enable inputs

SN54ALS138A, SN54AS138 . . . J PACKAGE SN74ALS138A, SN74AS138 . . . D OR N PACKAGE (TOP VIEW)

GND 8 9 Y6	A [ B [ C [ G2A [ G2B [ G1 [ Y7 [ GND ]	3 4 5 6 7	υ	16 15 14 13 12 11 10 9	V <sub>CC</sub>   Y0   Y1   Y2   Y3   Y4   Y5   Y6
------------	--	-----------------------	---	---	---

#### SN54ALS138A, SN54AS138...FK PACKAGE (TOP VIEW)



NC - No internal connection

reduce the need for external gates or inverters when expanding. A 24-line decoder can be implemented without external inverters and a 32-line decoder requires only one inverter. An enable input can be used as a data input for demultiplexing applications.

The SN54ALS138A and SN54AS138 are characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ALS138A and SN74AS138 are characterized for operation from 0°C to 70°C.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

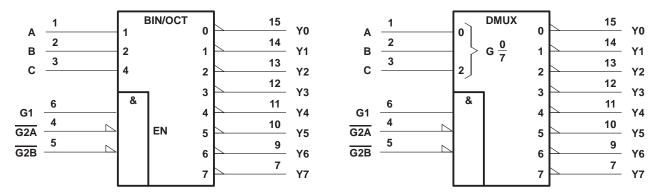
PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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					F	UNCTIO	N TABL	E					
		INP	JTS							ыне			
	ENABLE	E		SELECI	Γ	OUTPUTS							
G1	G2A	G2B	С	В	Α	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
Х	Н	Х	Х	Х	Х	н	Н	Н	Н	Н	Н	Н	Н
Х	Х	н	Х	Х	Х	н	Н	Н	Н	Н	Н	Н	Н
L	Х	Х	Х	Х	Х	н	Н	Н	Н	Н	Н	Н	Н
н	L	L	L	L	L	L	Н	Н	Н	Н	Н	Н	Н
н	L	L	L	L	Н	н	L	Н	Н	Н	Н	Н	Н
н	L	L	L	Н	L	н	Н	L	Н	Н	Н	Н	Н
н	L	L	L	Н	Н	н	Н	Н	L	Н	Н	Н	Н
н	L	L	н	L	L	н	Н	Н	Н	L	Н	Н	Н
н	L	L	н	L	Н	н	Н	Н	Н	Н	L	Н	Н
н	L	L	н	Н	L	н	Н	Н	Н	Н	Н	L	Н
н	L	L	н	Н	Н	н	Н	Н	Н	Н	Н	Н	L

### logic symbols (alternatives)<sup>†</sup>



 $^\dagger$  These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for the D, J, and N packages.



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15 Y0 14 - Y1 <u>13</u> Y2 Select 2 Inputs в <u>12</u> Y3 Data Outputs 11 Y4 3 С <u>10</u> Y5 9 \_\_\_\_ Y6 4 G2A 7 - Y7 Enable 5 G2B -Inputs 6 G1

Pin numbers shown are for the D, J, and N packages.

logic diagram (positive logic)



#### SDAS055E - APRIL 1982 - REVISED JULY 1996

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage, V <sub>CC</sub>	
Input voltage, V <sub>I</sub>	7 V
Operating free-air temperature range, T <sub>A</sub> : SN54ALS138A	-55°C to 125°C
SN74ALS138A	0°C to 70°C
Storage temperature range, T <sub>stg</sub>	-65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

#### recommended operating conditions

		SN5	54ALS13	8A	SN74ALS138A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Vcc	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage	2			2			V
VIL	Low-level input voltage			0.7			0.8	V
ЮН	High-level output current			-0.4			-0.4	mA
IOL	Low-level output current			4			8	mA
TA	Operating free-air temperature	-55		125	0		70	°C

# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED	TEO	TCONDITIONS	SNS	64ALS13	8A	SN7	4ALS13	8A	UNIT
PARAMETER	TES	T CONDITIONS	MIN	TYP‡	MAX	MIN	typ‡	MAX	UNIT
VIK	V <sub>CC</sub> = 4.5 V,	lj = -18 mA			-1.5			-1.5	V
VOH	V <sub>CC</sub> = 4.5 V,	$I_{OH} = -0.4 \text{ mA}$	V <sub>CC</sub> -2	2		V <sub>CC</sub> -2	2		V
Ve		$I_{OL} = 4 \text{ mA}$		0.25	0.4		0.25	0.4	V
VOL	V <sub>CC</sub> = 4.5 V	$I_{OL} = 8 \text{ mA}$					0.35	0.5	v
li	V <sub>CC</sub> = 5.5 V,	$V_{I} = 7 V$			0.1			0.1	mA
ЧΗ	V <sub>CC</sub> = 5.5 V,	V <sub>I</sub> = 2.7 V			20			20	μA
١ <sub>١L</sub>	V <sub>CC</sub> = 5.5 V,	$V_I = 0.4 V$			-0.1			-0.1	mA
۱ <sub>0</sub> §	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.25 V	-20		-112	-30		-112	mA
ICC	V <sub>CC</sub> = 5.5 V			5	10		5	10	mA

<sup>‡</sup> All typical values are at  $V_{CC} = 5 V$ ,  $T_A = 25^{\circ}C$ .

§ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, IOS.

#### switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	CL: RL:	2 = 4.5 V = 50 pF, = 500 Ω, = MIN to			UNIT
			SN54AL	S138A	SN74AL	S138A	
			MIN	MAX	MIN	MAX	
<sup>t</sup> PLH		Δον.Υ	2	28	5	22	20
<sup>t</sup> PHL	A, B, C	Any Y	6	22	6	18	ns
<sup>t</sup> PLH	G or G	Anv	2	22	3	17	ns
<sup>t</sup> PHL	6016	Any Y	4	21	4	17	115

 $\P$  For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.



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#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage, V <sub>CC</sub> Input voltage, V <sub>I</sub>	
Operating free-air temperature range, T <sub>A</sub> : SN54AS138SN74AS138	$-55^{\circ}$ C to $125^{\circ}$ C
Storage temperature range, T <sub>stg</sub>	-65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

#### recommended operating conditions

		SI	154AS13	8	SI	UNIT		
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Vcc	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage	2			2			V
VIL	Low-level input voltage			0.8			0.8	V
ЮН	High-level output current			-2			-2	mA
IOL	Low-level output current			20			20	mA
TA	Operating free-air temperature	-55		125	0		70	°C

# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED	TEST O	ONDITIONS	SN	54AS13	8	SN	174AS13	8	UNIT
PARAMETER	TEST C	JNDITIONS	MIN	TYP‡	MAX	MIN	typ‡	MAX	UNIT
VIK	$V_{CC} = 4.5 V,$	lj = -18 mA			-1.2			-1.2	V
VOH	$V_{CC} = 4.5 V \text{ to } 5.5 V,$	$I_{OH} = -2 \text{ mA}$	V <sub>CC</sub> -2			V <sub>CC</sub> -2	2		V
VOL	$V_{CC} = 4.5 V,$	I <sub>OL</sub> = 20 mA		0.35	0.5		0.35	0.5	V
lį	$V_{CC} = 5.5 V,$	$V_{I} = 7 V$			0.1			0.1	mA
ЧН	$V_{CC} = 5.5 V,$	V <sub>I</sub> = 2.7 V			20			20	μΑ
Ι <sub>ΙL</sub>	V <sub>CC</sub> = 5.5 V,	V <sub>I</sub> = 0.4 V			-0.5			-0.5	mA
١ <sub>O</sub> §	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.25 V	-30		-112	-30		-112	mA
Іссн	V <sub>CC</sub> = 5.5 V			12	17.5		12	17.5	mA
ICCL	V <sub>CC</sub> = 5.5 V			14	20		14	20	mA

<sup>‡</sup> All typical values are at  $V_{CC} = 5 V$ ,  $T_A = 25^{\circ}C$ .

§ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, IOS.



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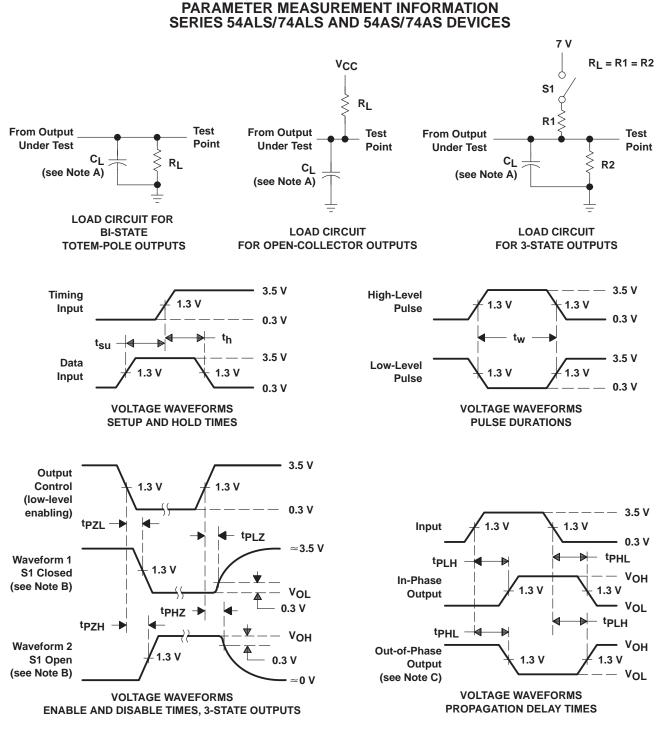
### switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)		= 50 pF = 500 Ω		V,	UNIT
			SN54A	\S138	SN74A	S138	
			MIN	MAX	MIN	MAX	
<sup>t</sup> PLH	A, B, C	Any Y	2	11	2	10	ns
<sup>t</sup> PHL	А, В, С		2	11	2	9.5	115
<sup>t</sup> PLH	G1	Any Y	2	11.5	2	10	ns
<sup>t</sup> PHL	61	Ally I	2	11	2	10	115
<sup>t</sup> PLH	G2	Δην.Υ	2	9	2	7.5	
<sup>t</sup> PHL	Gz	Any Y	2	10	2	8.5	ns

<sup>†</sup> For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

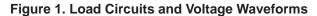


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NOTES: A. CL includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
   C. When measuring propagation delay items of 3-state outputs, switch S1 is open.
- D. All input pulses have the following characteristics: PRR  $\leq$  1 MHz, t<sub>r</sub> = t<sub>f</sub> = 2 ns, duty cycle = 50%.
- E. The outputs are measured one at a time with one transition per measurement.







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### **PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/ Ball Finish	MSL Peak Temp <sup>(3)</sup>	Samples (Requires Login)
5962-86866012A	ACTIVE	LCCC	FK	20	1	TBD	Call TI	Call TI	
5962-8686601FA	ACTIVE	CFP	W	16	1	TBD	Call TI	Call TI	
JM38510/37701B2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	
JM38510/37701BEA	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	
M38510/37701B2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	
M38510/37701BEA	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	
SN54ALS138AJ	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	
SN54AS138J	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	
SN74ALS138AD	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ALS138ADE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ALS138ADG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ALS138ADR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ALS138ADRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ALS138ADRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ALS138AN	ACTIVE	PDIP	Ν	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SN74ALS138ANE4	ACTIVE	PDIP	Ν	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SN74ALS138ANSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ALS138ANSRE4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ALS138ANSRG4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AS138D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AS138DE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	



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Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/ Ball Finish	MSL Peak Temp <sup>(3)</sup>	Samples (Requires Login)
SN74AS138DG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AS138DR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AS138DRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AS138DRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AS138N	ACTIVE	PDIP	Ν	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SN74AS138N3	OBSOLETE	PDIP	Ν	16		TBD	Call TI	Call TI	
SN74AS138NE4	ACTIVE	PDIP	Ν	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SN74AS138NSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AS138NSRE4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AS138NSRG4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SNJ54ALS138AFK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	
SNJ54ALS138AJ	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	
SNJ54ALS138AW	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type	
SNJ54AS138FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	
SNJ54AS138J	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	

<sup>(1)</sup> The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.



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Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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#### OTHER QUALIFIED VERSIONS OF SN54ALS138A, SN54AS138, SN74ALS138A, SN74AS138 :

• Catalog: SN74ALS138A, SN74AS138

• Military: SN54ALS138A, SN54AS138

NOTE: Qualified Version Definitions:

- Catalog TI's standard catalog product
- Military QML certified for Military and Defense Applications

### TAPE AND REEL INFORMATION





### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device		Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ALS138ADR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74ALS138ANSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74AS138DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74AS138NSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1



# PACKAGE MATERIALS INFORMATION

19-Mar-2008



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ALS138ADR	SOIC	D	16	2500	333.2	345.9	28.6
SN74ALS138ANSR	SO	NS	16	2000	346.0	346.0	33.0
SN74AS138DR	SOIC	D	16	2500	333.2	345.9	28.6
SN74AS138NSR	SO	NS	16	2000	346.0	346.0	33.0

J (R-GDIP-T\*\*) 14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F16)

CERAMIC DUAL FLATPACK



- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only.
  - E. Falls within MIL STD 1835 GDFP1-F16 and JEDEC MO-092AC



LEADLESS CERAMIC CHIP CARRIER

FK (S-CQCC-N\*\*) 28 TERMINAL SHOWN



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

- C. This package can be hermetically sealed with a metal lid.
- D. Falls within JEDEC MS-004



# N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



NOTES:

- A. All linear dimensions are in inches (millimeters).B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- $\triangle$  The 20 pin end lead shoulder width is a vendor option, either half or full width.



D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AC.



4211283-4/D 06/11

# D (R-PDSO-G16) PLASTIC SMALL OUTLINE Stencil Openings (Note D) Example Board Layout (Note C) -16x0,55 - 14x1,27 -14x1,27 16x1,95 4,80 4,80 Example Non Soldermask Defined Pad Example Pad Geometry (See Note C) 0,60 Example 2,00 Solder Mask Opening

(See Note E)

NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

← 0,07 All Around

- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



### MECHANICAL DATA

### PLASTIC SMALL-OUTLINE PACKAGE

#### 0,51 0,35 ⊕0,25⊛ 1,27 8 14 0,15 NOM 5,60 8,20 5,00 7,40 $\bigcirc$ Gage Plane ₽ 0,25 7 1 1,05 0,55 0°-10° Δ 0,15 0,05 Seating Plane — 2,00 MAX 0,10PINS \*\* 14 16 20 24 DIM 10,50 10,50 12,90 15,30 A MAX A MIN 9,90 9,90 12,30 14,70 4040062/C 03/03

NOTES: A. All linear dimensions are in millimeters.

NS (R-PDSO-G\*\*)

**14-PINS SHOWN** 

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



#### **IMPORTANT NOTICE**

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