SDLS166 OCTOBER 1976 - REVISED MARCH 1988

Supply Voltage and Ground on Corner Pins To Simplify P-C Board Layout

description

The SN54LS375 and SN74LS375 bistable latches are electrically and functionally identical to the SN54LS75 and SN74LS75, respectively. Only the arrangement of the terminals has been changed in the SN54LS375 and SN74LS375.

These latches are ideally suited for use as temporary storage for binary information between processing units and input/output or indicator units. Information present at a data (D) input is transferred to the Q output when the enable (C) is high and the Q output will follow the data input as long as the enable remains high. When the enable goes low, the information (that was present at the data input at the time the transition occurred) is retained at the Q output until the enable goes high.

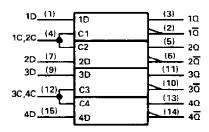
All inputs are diode-clamped to minimize transmissionline effects and simplify system design. The SN54LS375 is characterized for operation over the full military temperature range of - 55°C to 125°C; SN74LS375 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE (EACH LATCH) INPUTS OUTPUTS D G Q ā I ī Ħ н н н $\underline{\sigma}^{\vec{0}}$ σ^{0} L

H = high lever, L = low level, X = irrelevant

 $Q_{\overline{Q}}$ = the level of Q before the high-to low transition of C.

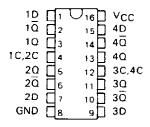
logic symbol[†]



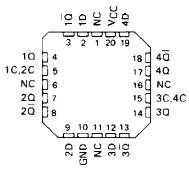
[†]This symbol is in accordance with ANSI/IEEE Std. 91-1984 and JEC Publication 617-12

Pin numbers shown are for D, J, N, and W packages.

SN54LS375 . . . J OR W PACKAGE SN74LS375 . . . D OR N PACKAGE (TOP VIEW)

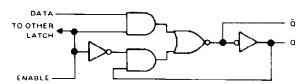


SN54LS375 . . . FK PACKAGE (TOP VIEW)

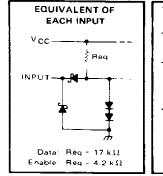


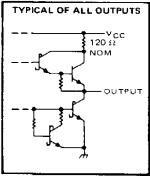
NC - No internal connection

logic diagram (each latch)



schematics of inputs and outputs





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SN54LS375, SN74LS375 4-BIT BISTABLE LATCHES

olute maximum rati <mark>ngs over oper</mark> a	ting fr ee -air	tem	pe	ratı	ure	ran	ıge	(ur	1le:	SS C	th	BIV	vis	n	ote	d)			
Supply voltage, VCC (see Note 1) .											. ,							, .	
Input voltage				,															
Operating free air temperature range:	SN54L5375																-5	5°C	to 12
	SN74LS375																	0°4	C to 7
Storage temperature range				,													-6	5°C	to 15

recommended operating conditions

			SN54LS375		SN74LS375			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	7 01311
Vcc	Supply voltage	4.5	5	5.5	4,75	5	5.25	V
VIH	High-lever input voltage	2			2			V
VIL	Low-level input voltage			0.7			0.8	V
ЮН	High-level autput current			~ 0.4		_	- 0.4	mA
^I OL	Low-level output current			4			8	mΑ
^t w	Width of enabling pulse	20		W	20			ns
:setup	Setup time	20			20	-		ns
thold	Hold time	0	 -		0			пѕ
TA	Operating free-air temperature	- 55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED.	=	rights t		SN54LS	375					
PARAMETER	TEST CONDITIONS T			MIN	TYP ‡	MAX	MIN	TYP‡	MAX	UNIT
ViK	VCC = MIN,	1 ₁ = −18 mA				-1.5			- 1.5	V
VOH	V _{CC} ≈ MIN, l _{OH} ≈ = 0.4 m.		VIL = MAX	2.5	3.5	•	2.7	3.5	-	V
37 -	V _{CC} = MIN,	V _{IH} = 2 V,	IOL = 4 mA		0.25	0.4		0.25		
VOL VI	VIL = MAX		IOL = 8 mA					0.35	0.5	1 *
	V _{CC} = MAX.	V 7 V	D input			0.1			0.1	mΑ
4	VCC - MAA.	V - / V	Cinput			0.4			0.4	1 "
1	V _{CC} = MAX	V ₁ = 2.7 V	Dinput			20			20	1
ΉΗ	ACC = MAX	V - 2.7 U	Cinput			80			80	Αμ.
	W AAA V	17 = 0.417	D input			- 0.4			- 0.4	mA
l _{IE}	V _{CC} = MAX,	V = 0.4 V	Cinput			- 16			- 1.6	1 '''^
105;	V _{CC} - MAX			-20		- 100	-20		- 100	mΑ
¹CC	VCC = MAX.	See Note 2			6.3	12		6.3	12	mA

 $[\]dagger$ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

switching characteristics, VCC = 5 V, TA = 25°C (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN TYP	MAX	UNIT
¹ PL H	D	0		15	27	D.
1PHL .				9	17	ns
tpLH	D	ā	$R_L = 2 k \Omega$, $C_L = 15 pF$	12	20	200
tPHL			7 L 2 K42. CL - 13 B1	7	15	ns
†PLH	 C			15	27	
[†] PHL				14	25	ns
1PLH	C	ā		16	30	
[†] PHL				7	15	ns

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.



[‡] All typical values are at V_{CC} = 5 V, T_A = 25 C.

Not more than one output should be shorted at a time.

NOTE 2 ICC is tested with all inputs grounded and all outputs open.



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PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
SN54LS375J	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	Purchase Samples
SN74LS375D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples
SN74LS375D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples
SN74LS375DE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples
SN74LS375DE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples
SN74LS375DG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples
SN74LS375DG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples
SN74LS375J	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI	Samples Not Availal
SN74LS375J	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI	Samples Not Availal
SN74LS375N	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	Purchase Samples
SN74LS375N	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	Purchase Samples
SN74LS375N3	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI	Samples Not Availal
SN74LS375N3	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI	Samples Not Availal
SN74LS375NE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	Purchase Samples
SN74LS375NE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	Purchase Samples
SN74LS375NSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples
SN74LS375NSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples
SN74LS375NSRE4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples
SN74LS375NSRE4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples
SN74LS375NSRG4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples
SN74LS375NSRG4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples



www.ti.com 28-Aug-2010

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
SNJ54LS375FK	OBSOLETE	LCCC	FK	20		TBD	Call TI	Call TI	Samples Not Available
SNJ54LS375FK	OBSOLETE	LCCC	FK	20		TBD	Call TI	Call TI	Samples Not Available
SNJ54LS375J	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	Purchase Samples
SNJ54LS375J	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	Purchase Samples
SNJ54LS375W	OBSOLETE			16		TBD	Call TI	Call TI	Samples Not Available
SNJ54LS375W	OBSOLETE			16		TBD	Call TI	Call TI	Samples Not Available

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL. Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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OTHER QUALIFIED VERSIONS OF SN54LS375, SN74LS375:

Catalog: SN74LS375





28-Aug-2010

Military: SN54LS375

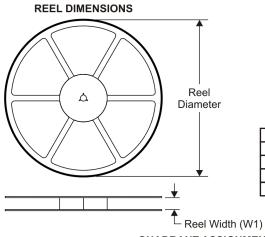
NOTE: Qualified Version Definitions:

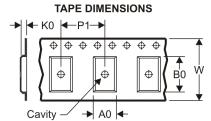
- Catalog TI's standard catalog product
- Military QML certified for Military and Defense Applications

PACKAGE MATERIALS INFORMATION

www.ti.com 23-Jul-2010

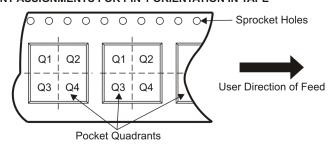
TAPE AND REEL INFORMATION





_		
	Α0	Dimension designed to accommodate the component width
		Dimension designed to accommodate the component length
	K0	Dimension designed to accommodate the component thickness
	W	Overall width of the carrier tape
Γ	P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing			Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LS375NSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1

PACKAGE MATERIALS INFORMATION

www.ti.com 23-Jul-2010



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LS375NSR	SO	NS	16	2000	346.0	346.0	33.0

14 LEADS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a metal lid.
- D. Falls within JEDEC MS-004



N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- The 20 pin end lead shoulder width is a vendor option, either half or full width.



D (R-PDS0-G16)

PLASTIC SMALL OUTLINE



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AC.



MECHANICAL DATA

NS (R-PDSO-G**)

14-PINS SHOWN

PLASTIC SMALL-OUTLINE PACKAGE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



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